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PATENT APPLICATION

ATTORNEY DOCKET NO. 10012773-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Richard W. Adkisson

Confirmation No.: 7649

Application No.: 09/887,797

Examiner: Juan A. Torres

Filing Date: June 22, 2001

Group Art Unit: 2631

Title: SYNC Pulse Compensation and Regeneration in a Clock Synchronizer Controller

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on August 15, 2005.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $500.00. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Number of pages: 35

Typed Name: Shreen K. Danamraj

Signature: /SKDanamraj/

Respectfully submitted,

Richard W. Adkisson

By /SKDanamraj/

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DOCKET NO.: 10012773-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of:	§	
	§	
Richard W. Adkisson	§	Confirmation No.: 7649
	§	
Application No.: 09/887,797	§	Art Unit: 2631
	§	
Filed: June 22, 2001	§	Examiner: Juan A. Torres

For: SYNC PULSE COMPENSATION AND REGENERATION IN A CLOCK SYNCHRONIZER CONTROLLER

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I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office on OCTOBER 14, 2005.

Shreen R. Danamraj

Dear Sir:

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Pursuant to 37 C.F.R. §41.37, Applicant (hereinafter "Appellant") hereby submits an appeal brief in the above-captioned patent application within the requisite time from the date of filing of the Notice of Appeal which was filed on August 15, 2005.

This appeal is from the decision of Examiner Juan A. Torres, Art Unit 2631, rejecting claims 1-12 and 14-19 in the present

patent application, as set forth in the Final Office Action dated June 14, 2005.

I. REAL PARTY IN INTEREST

The real party in interest of the present patent application is Hewlett-Packard Development Company, a Texas Limited Liability Partnership having its principal place of business in Houston, Texas.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any other prior and/or pending appeals, interferences, or judicial proceedings which may be related to, directly affect or be directly affected by or otherwise have a bearing on the Board's decision in this pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 are currently pending, of which claims 1, 10, 14, and 20 are in independent form.

Claims 1-12 and 14-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over a number of references applied in various combinations: (i) claims 1-3, 14-16, and 19 over U.S. Patent No. 5,450,458 to Price et al. (the *Price* reference) in view of U.S. Patent No. 6,622,255 to Kurd et al. (the *Kurd* reference);

(ii) claim 4 over the *Price* and *Kurd* references in further view of U.S. Patent No. 5,054,020 to Meagher (the *Meagher* reference); (iii) claims 5-9 and 17-18 over the *Price* and *Kurd* references in further view of U.S. Patent No. 6,396,322 to Kim et al. (the *Kim* reference); (iv) claims 10 and 12 over the *Price* and *Meagher* references; (v) claim 11 over the *Price* and *Meagher* references in further view of U.S. Patent No. 5,256,994 to Langendorf (the *Langendorf* reference); and (vi) claim 12 over the *Price* and *Meagher* references in further view of U.S. Patent No. 6,516,362 to Magro et al. (the *Magro* reference).

Claim 13 is being objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 20 is allowed.

Claims 1-12 and 14-19 are on appeal.

IV. STATUS OF AMENDMENTS

No substantive amendments have been made or requested since the mailing of the Final Office Action and amendments submitted prior to the Final Office Action have been entered. Set forth below is a synopsis of the chronology:

A First Office Action was mailed on October 6, 2004 indicating that the original claims 1-19 were allowable over the art of record. This First Office Action included certain claim objections as well as objections to the disclosure.

Appellant filed a Response on November 16, 2004 with traversal as to the objections raised in the October 6, 2004 Office Action.

A Second, Non-Final Office Action was mailed on January 11, 2005 in which claims 1-12 and 14-19 were rejected under 35 U.S.C. §103(a) as being unpatentable over a number of newly discovered references. Claim 13 was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Appellant filed a Response on April 11, 2005 with traversal and argument as to the art-based rejections raised in the January 11, 2005 Office Action. Further, Appellant added a new claim, claim 20, including the allowable subject matter of claim 13.

A Final Office Action was mailed on June 14, 2005 in which the art-based rejections of claims 1-12 and 14-19 raised in the previous Office Action were maintained.

Appellant filed a Notice of Appeal on August 15, 2005 in response to the Final Office Action of June 14, 2005.

A copy of the claims involved in this appeal is attached hereto as an Appendix.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A concise explanation of the subject matter defined in each of the independent claims is set forth in this Section, including appropriate references to the specification, e.g., by page and line number, reference numerals in drawings, etc. These specific references are examples of particular elements of the drawings for certain embodiments of the claimed invention, and the claims are not limited solely to the elements corresponding to the applied reference numerals.

Independent claim 1 is directed to an embodiment of a SYNC pulse compensation apparatus (see, e.g., FIGURE 8A and related description in the specification at page 17, line 16 through page 19, line 28; see also SUMMARY at page 3, lines 1-19). A sampling compensation circuit (801) included in the SYNC pulse compensation apparatus is operable to condition a SYNC pulse signal (108), wherein the SYNC pulse signal (108) is based on a predetermined temporal relationship between a first clock signal (104) operable to clock a first circuit portion (114) and a second clock signal (105) operable to clock a second circuit portion (112) (see, e.g.,

FIGURE 1 and related description in the specification at page 6, lines 5-20). A jitter cycle delay compensation circuit (813) coupled to the sampling compensation circuit (801) operates to tap the SYNC pulse signal after a predetermined delay based on a skew difference between the first and second clock signals (104, 105) (see, e.g., specification at page 18, lines 12-31).

Independent claim 10 is directed to an embodiment of a SYNC pulse compensation method (see, e.g., FIGURE 8A and related description in the specification at page 17, line 16 through page 19, line 28; see also specification at page 16, line 25 through page 17, line 15 and SUMMARY at page 3, lines 1-19). The method comprises sampling a SYNC pulse signal (108) (see, e.g., specification at page 17, lines 30-31), which SYNC pulse signal (108) is generated based on a predetermined temporal relationship between a first clock signal (104) operable to clock a first circuit portion (114) and a second clock signal (105) operable to clock a second circuit portion (112) (see, e.g., FIGURE 1 and related description in the specification at page 6, lines 5-20; see also FIGURE 7, step 704). If the SYNC pulse signal is sampled to contain an anomalous condition during a predetermined period (see, e.g., specification at page 16, line 31 through page 17, line 15), such anomalous condition is removed by activating appropriate SYNC

correct control logic (803) (see, e.g., specification at page 17, line 31 through page 18, line 11).

Independent claim 14 is directed to an embodiment of a SYNC pulse compensation method (see, e.g., FIGURE 8A and related description in the specification at page 17, line 16 through page 19, line 28; see also specification at page 16, line 25 through page 17, line 15 and SUMMARY at page 3, lines 1-19). The method comprises sampling a SYNC pulse signal (108) (see, e.g., specification at page 17, lines 30-31), which SYNC pulse signal (108) is generated based on a predetermined temporal relationship between a first clock signal (104) operable to clock a first circuit portion (114) and a second clock signal (105) operable to clock a second circuit portion (112) (see, e.g., FIGURE 1 and related description in the specification at page 6, lines 5-20; see also FIGURE 7, step 704). A clock state indicative of a phase difference between the first and second clock signals (104, 105) is determined (see, e.g., FIGURE 4 and related description in the specification at page 11, line 15 through page 12, line 2; see also specification at page 10, lines 4-10). The SYNC pulse signal is re-positioned based on the clock state (see, e.g., specification at page 17, line 15 through page 18, line 11). If the SYNC pulse signal is out-of-phase by a predetermined amount with respect to

the first clock signal (104), the SYNC pulse signal is delayed based on the clock state (see, e.g., specification at page 18, line 12 through page 19, line 11).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(i) Claims 1-3, 14-16, and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,450,458 to Price et al. (the *Price* reference) in view of U.S. Patent No. 6,622,255 to Kurd et al. (the *Kurd* reference).

(ii) Claim 4 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the *Price* and *Kurd* references in further view of U.S. Patent No. 5,054,020 to Meagher (the *Meagher* reference).

(iii) Claims 5-9 and 17-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the *Price* and *Kurd* references in further view of U.S. Patent No. 6,396,322 to Kim et al. (the *Kim* reference).

(iv) Claims 10 and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the *Price* and *Meagher* references.

(v) Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the *Price* and *Meagher* references in further view of U.S. Patent No. 5,256,994 to Langendorf (the *Langendorf* reference).

(vi) Claim 12 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the *Price* and *Meagher* references in further view of U.S. Patent No. 6,516,362 to Magro et al. (the *Magro* reference).

VII. ARGUMENT

(i) Claims 1-3, 14-16, and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,450,458 to Price et al. in view of U.S. Patent No. 6,622,255 to Kurd et al.

(A) Argument with respect to Base Claim 1 and Dependent Claims 2 and 3 Depending Therefrom

The following comments were provided in the pending Final Office Action in particular reference to the §103 rejections of the base claim 1:

> As per claim 1 Price discloses a sampling compensation circuit operable to condition a SYNC pulse signal, wherein said SYNC pulse signal is based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67). Price doesn't disclose a jitter cycle delay compensation circuit coupled to said sampling compensation circuit, said jitter cycle delay compensation circuit operating to tap said SYNC pulse signal after a predetermined delay based on a skew difference between said first and second clock signals. Kurd discloses a jitter cycle delay compensation circuit coupled to said sampling compensation circuit, said jitter cycle delay compensation circuit operating to tap said SYNC pulse signal after a predetermined delay based on a skew difference between said first and second clock

> signals (figure 6 column 5 lines 41-44). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18). Therefore, it would have been obvious to combine Price and Kurd to obtain the invention as specified in claim 1.

As set forth in the base claim 1, an embodiment of the present invention is directed to a SYNC pulse compensation apparatus that comprises, *inter alia*, a **sampling compensation circuit operable to condition** a SYNC pulse signal. The *Price* reference is directed to a digital information handling system that employs subsystems operating with different clock frequencies and which are capable of transferring data between one another. The applied language of the *Price* reference at column 9, lines 37-42 and lines 65-67 does not teach, suggest or even remotely allude to a sampling compensation circuit operable to condition a SYNC signal. Rather, it merely discloses that a first synchronization circuit 136 generates a synchronization signal called SYNC READY to synchronize data transfer from Memory Controller 126 in a second subsystem clock environment to System Processor 124 in a first subsystem via System Processor Bus 128. See *Price* at column 9, lines 37-42. Appellant respectfully submits that generation of SYNC READY signal does not

anticipate or suggest **conditioning** a SYNC pulse as claimed. As set forth in the specification of the present patent application, **conditioning** of the SYNC pulse is performed by the sampling compensation circuit (801) in order to remove certain anomalus conditions in the SYNC pulse, e.g., a lost SYNC pulse, a duplicate pulse condition, etc. See, e.g., specification at page 17, line 16 to page 18, line 11.

On the other hand, the language at column 9, lines 65-67 of Price provides a description of a clock generation circuit 118. See FIGURE 8. This description reads:

> Clock Generation Circuit 118 produces multiple clock signals having different frequencies and a fixed predetermined timing relationship. Clock Generation Circuit 118 also produces multiple synchronization pulses which correspond to the timing relationship of the clock signals it produces.

Appellant respectfully submits that the clock generation circuit 118 of *Price* does not teach or suggest the claimed sampling compensation circuit (801) operable to remove certain anomalus conditions in **a SYNC pulse**. Rather, at best, the clock generation circuit 118 of *Price* is merely operable to produce **multiple** synchronization pulses, SYNC PULSE 1 and SYNC PULSE 2. Appellant respectfully contends that mere **production** of one or multiple SYNC

pulses is not anticipatory or suggestive of **conditioning** of a SYNC pulse as claimed in the base claim 1.

Moreover, as admitted in the pending Office Action, the *Price* reference does not disclose a jitter cycle delay compensation circuit (813) as recited in the base claim 1. Application of the *Kurd* reference is of no avail, however, when applied as a secondary reference in combination with the *Price* reference in order to provide a basis for obviousness. It is well known that to establish a *prima facie* case of obviousness, a prerequisite condition is that the combined references must teach or suggest all the claim limitations. See MPEP §2143. Appellant respectfully contends that the applied art does not teach or suggest all the claim limitations which include, *inter alia*, (i) a sampling compensation circuit operable to condition a SYNC pulse signal; and (ii) a jitter cycle delay compensation circuit coupled to the sampling compensation circuit, wherein the jitter cycle delay compensation circuit **operates to tap the SYNC pulse** signal after a predetermined delay based on a skew difference between first and second clock signals. The *Kurd* reference is directed to digital clock skew detection and phase alignment between two digital clock signals that are copies of each other. See *Kurd* at column 1, lines 11-24. As such, there is no teaching or suggestion whatsoever in

the *Kurd* reference with regard to a SYNC sampling compensation circuit operable to **condition a SYNC pulse signal** as claimed. FIGURE 6 of the *Kurd* reference shows a circuit schematic of an application of a skew detection circuit for minimizing skew between different clock domains. Two separate frequency control circuits are provided, PLL1 606 and PLL2 608, which provide output clocks of different frequencies. Column 5, lines 41-47. A reference clock is split into two by a programmable delay circuit 504 and fed to separate inputs of the two PLLs. Each PLL adjusts the phase and/or frequency of its output signal to match that of the reference input. Column 5, lines 47-63. In other words, the operation of the skew detection circuit does not involve tapping of a SYNC pulse signal at all. Appellant respectfully submits that the skew detection circuit of the *Kurd* reference does not even remotely allude to the claimed jitter cycle delay compensation circuit that is coupled to a SYNC sampling compensation circuit, wherein the jitter cycle delay compensation circuit **operates to tap** a conditioned SYNC pulse signal at different tap points as currently claimed. Accordingly, it is respectfully submitted that the combination of the *Price* and *Kurd* references does not teach or suggest all the claim limitations as required under MPEP §2143.

Furthermore, it is yet another requirement that there must be a reasonable expectation of success in order to establish obviousness. See MPEP §2143. Appellant respectfully submits that the pending Final Office Action does not appear to set forth the factual support required for establishing that there is a reasonable expectation of success when the *Price* and *Kurd* references are to be combined for purposes of MPEP §§2142-2143.

At least for the foregoing reasons, Appellant respectfully submits that the base claim 1 is allowable over the *Price* and *Kurd* references. Dependent claims 2 and 3 depend from the base claim 1 and introduce additional limitations therein. Accordingly, these two dependent claims are also allowable over the *Price* and *Kurd* references based on the argument set forth above.

(B) Argument with respect to Base Claim 14 and Dependent Claims 15, 16, and 19 Depending Therefrom

The following comments were provided in the pending Final Office Action in particular reference to the §103 rejection of the base claim 14::

> As per claim 14 Price (US 5450458) discloses sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67); determining a clock state indicative of a phase difference between said first and second clock

> signals (figure 7 block 74 column 7 lines 46-48); Price doesn't disclose re-positioning the SYNC pulse signal based on said clock state and if the SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state. Kurd discloses re-positioning the SYNC pulse signal based on said clock state and if the SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state (figure 5 column 5 lines 10-16). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the delay system circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18). Therefore, it would have been obvious to combine Price and Kurd to obtain the invention as specified in claim 14.

Appellant respectfully submits that, first of all, the applied language of the *Price* reference at column 9, lines 37-42 and lines 65-67 does not teach, suggest or even remotely allude to **sampling a SYNC pulse signal**. Rather, as discussed hereinabove, the applied language merely discloses **production** of multiple synchronization pulses. Further, the applied language at column 7, lines 46-48 of *Price* does not teach, suggest or allude to determining a clock state indicative of a phase difference between first and second clock signals. Rather, a frequency synthesizer with waveform sequencer 74 is described therein which is in data communication with CPU 58 via a First SYNC bus 78 and in data communication with

Memory Controller 62 via a Second SYNC bus 82. See FIGURE 7 of *Price*. The function of the waveform sequencer is further described in reference to a particular embodiment of waveform sequencer 132 shown in FIGURE 8. As shown therein, waveform sequencer 132 generates multiple frequency clocks, CLK 1 and CLK 2, as well as multiple SYNC pulses. See also column 9, lines 15-30 of *Price*. Appellant accordingly submits that there is simply no teaching or suggestion in the applied language with respect to **determining a clock state** indicative of a phase difference between first and second clock signals as recited in the base claim 14.

On the other hand, application of the *Kurd* reference does not cure the deficiencies of the *Price* reference when applied in combination therewith. As argued above, *Kurd* is not even concerned with sampling a SYNC signal. Additionally, although it is provided in *Kurd* that an adjusted reference clock is obtained by delaying a reference clock signal in accordance with a first count (column 5, lines 10-16), there is no teaching or suggestion with respect to **determining a clock state and re-positioning a SYNC pulse signal based on the clock state**. Accordingly, even if the two references were to be combined, they fail to teach or suggest all the limitations of the base claim 14.

Further, Appellant respectfully submits, as before, that the pending Final Office Action does not appear to set forth the factual support required for establishing that there is a reasonable expectation of success when the *Price* and *Kurd* references are to be combined for purposes of MPEP §§2142-2143.

At least for the foregoing reasons, Appellant respectfully submits that the base claim 14 is allowable over the *Price* and *Kurd* references. Dependent claims 15, 16, and 19 depend from the base claim 14 and introduce additional limitations therein. Accordingly, these three dependent claims are also allowable over the *Price* and *Kurd* references based on the argument set forth above.

(ii) Claim 4 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the *Price* and *Kurd* references in further view of U.S. Patent No. 5,054,020 to Meagher.

Dependent claim 4 ultimately depends from the base claim 1 via intervening dependent claim 2, and introduces additional limitations accordingly. As argued above, the combination of *Price* and *Kurd* references is deficient for purposes of maintaining obviousness-based rejection of the base claim 1 or the dependent claim 2. Application of the *Meagher* reference (which is discussed

separately hereinbelow), however, is of no avail in terms of curing the deficiencies of the combination of *Price* and *Kurd* references. Appellant respectfully submits that the entire combination of *Price*, *Kurd* and *Meagher* references does not suggest or allude to at least the following limitations: (i) a sampling compensation circuit operable to condition a SYNC pulse signal; and (ii) a jitter cycle delay compensation circuit coupled to the sampling compensation circuit, wherein the jitter cycle delay compensation circuit operates to tap the SYNC pulse signal after a predetermined delay based on a skew difference between first and second clock signals. Accordingly, claim 4 is allowable over the applied combination of references.

(iii) Claims 5-9 and 17-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the *Price* and *Kurd* references in further view of U.S. Patent No. 6,396,322 to Kim et al.

(A) Argument with respect to Claims 5-9

Dependent claims 5-9 ultimately depend from the base claim 1 and introduce additional limitations accordingly. As argued above, the combination of *Price* and *Kurd* references is deficient for purposes of maintaining obviousness-based rejection of the base claim 1. Application of the *Kim* reference, which is directed to a

delay locked loop of a memory device, however, is of no avail in terms of curing the deficiencies of the combination of *Price* and *Kurd* references. Appellant respectfully submits that the entire combination of *Price*, *Kurd* and *Kim* references does not suggest or allude to at least the following limitations: (i) a sampling compensation circuit operable to condition a SYNC pulse signal; and (ii) a jitter cycle delay compensation circuit coupled to the sampling compensation circuit, wherein the jitter cycle delay compensation circuit operates to tap the SYNC pulse signal after a predetermined delay based on a skew difference between first and second clock signals. Accordingly, claims 5-9 are allowable over the applied combination of references.

(B) Argument with respect to Claims 17-18

Dependent claims 17 and 18 ultimately depend from the base claim 14 and introduce additional limitations accordingly. As argued above, the combination of *Price* and *Kurd* references is deficient for purposes of maintaining obviousness-based rejection of the base claim 14. Again, Appellant respectfully submits that the entire combination of *Price*, *Kurd* and *Kim* references does not suggest or allude to at least the following features: (i) sampling a SYNC pulse signal; and (ii) determining a clock state and re-positioning the SYNC pulse signal based on the clock state.

Accordingly, claims 17 and 18 are allowable over the applied combination of references.

(iv) Claims 10 and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the *Price* and *Meagher* references.

The following comments were provided in the pending Final Office Action in particular reference to the §103 rejection of the base claim 10:

> As per claim 10 Price discloses a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67). Price doesn't disclose that when the signal contains an anomalous condition during a predetermined time period, removing said anomalous condition by activating appropriate SYNCH correct control logic. It is very well known and Meagher discloses that when the signal contains an anomalous condition during a predetermined time period, removing said anomalous condition by activating appropriate SYNCH correct control logic (figure 2, column 2 lines 30-31). Price and Meagher teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate synchronization technique disclosed by Meagher with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to prevent the lost of synchronization avoiding the use of a sequence of predetermined zeros (Meagher figure 2, column 2 lines 24-55). Therefore, it would have been obvious to combine Price and Meagher to obtain the invention as specified in claim 10.

As currently constituted, the base claim 10 involves, *inter alia*, (i) **sampling a SYNC pulse signal** generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion; and (ii) **if the SYNC pulse signal is sampled to contain an anomalous condition during a predetermined time period, removing the anomalous condition by activating appropriate SYNC correct control logic.** As discussed in detail hereinabove, the applied language of the *Price* reference at column 9, lines 37-42 and lines 65-67 does not teach, suggest or even remotely allude to **sampling a SYNC pulse signal.** Rather, the applied language merely discloses **production** of multiple synchronization pulses. Further, the *Price* reference does not disclose or suggest removing of any anomalous condition in the sampled SYNC pulse signal by activating appropriate SYNC correct control logic (803), as currently claimed in the base claim 10.

Appellant respectfully traverses the official notice taken with respect to the claimed feature that recites "if said SYNC pulse signal is sampled to contain an anomalous condition, removing said anomalous condition by activating appropriate SYNC correct control logic". To the extent the *Meagher* reference is relied upon as documentary evidence for this official notice as per MPEP

§2144.03, there is no record as to sampling a SYNC pulse signal or as to what constitutes an anomalous condition therein.

The *Meagher* reference is directed to a scheme for converting an incoming asynchronous data signal into an outgoing synchronous data signal and vice versa in a data communication system such as the T1 carrier system that operates with a DS-1 signal. See *Meagher* at column 1, lines 9-41. In order to maintain maximum throughput on a T1 line, the one's density requirement must be complied with. Accordingly, a channel bank's Line Interface Unit (LIU) provides one's density control by inserting a one in bit 2 whenever the other bits in the DS word are all zeros. See *Meagher* at column 2, lines 30-31.

Appellant respectfully submits that insertion of a one to maintain a certain density requirement in a T1 data communication system does not suggest or allude to sampling a SYNC pulse signal and **removing an anomalous condition therein by activating appropriate SYNC correct control logic**. Accordingly, the combined teachings of the *Price* and *Meagher* references fail to teach or suggest all the limitations of the base claim 10 as required under MPEP §2143. Additionally, even if the teachings of the applied references were to be combined, there cannot be a reasonable expectation of successfully obtaining Appellant's claimed invention

because the operating conditions of a T1 transmission line (in the *Meagher* reference) are vastly different from those of the asynchronous subsystems within a computer as disclosed in the *Price* reference.

Further, at any rate, Appellant respectfully submits that the pending Final Office Action does not appear to set forth the factual support required for establishing that there is a reasonable expectation of success when the *Price* and *Meagher* references are to be combined for purposes of MPEP §§2142-2143.

At least for the foregoing reasons, Appellant respectfully submits that the base claim 10 is allowable over the *Price* and *Meagher* references. Dependent claim 12 depends from the base claim 10 and introduces additional limitations therein. Accordingly, this dependent claim is also allowable over the *Price* and *Meagher* references based on the argument set forth above.

(v) Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the *Price* and *Meagher* references in further view of U.S. Patent No. 5,256,994 to Langendorf.

Dependent claim 11 depends from the base claim 10 and introduces additional limitations accordingly. As argued above, the combination of *Price* and *Meagher* references is deficient for

purposes of maintaining obviousness-based rejection of the base claim 10. Application of the *Langendorf* reference (which is directed to a programmable secondary clock generator), however, is of no avail in terms of curing the deficiencies of the combination of *Price* and *Meagher* references. Appellant respectfully submits that the entire combination of *Price*, *Meagher* and *Langendorf* features: (i) a sampling a SYNC pulse signal; and (ii) if the SYNC pulse signal is sampled to contain an anomalous condition during a predetermined time period, removing the anomalous condition by activating appropriate SYNC correct control logic. Accordingly, claim 11 is allowable over the applied combination of references.

(vi) Claim 12 stands rejected under 35 U.S.C. §103(a) as being unpatentable over the *Price* and *Meagher* references in further view of U.S. Patent No. 6,516,362 to Magro et al.

Dependent claim 12 depends from the base claim 10 and introduces additional limitations accordingly. As argued above, the combination of *Price* and *Meagher* references is deficient for purposes of maintaining obviousness-based rejection of the base claim 10 as well as the dependent claim 12. To the extent this separate rejection of claim 12 is proper and consistent at all with its prior rejection (as set forth in item (iv)), application of the

Magro reference (which is directed to synchronizing data between differing clock domains) is of no avail in terms of curing the deficiencies of the combination of *Price* and *Meagher* references. Appellant respectfully submits that the entire combination of *Price, Meagher* and *Magro* references does not suggest or allude to at least the following features: (i) a sampling a SYNC pulse signal; and (ii) if the SYNC pulse signal is sampled to contain an anomalous condition during a predetermined time period, removing the anomalous condition by activating appropriate SYNC correct control logic. Accordingly, claim 12 is allowable over the applied combination of references.

DOCKET NO.: 10012773-1

CONCLUSION

In view of the foregoing discussion, Appellant respectfully submits that the rejection of the pending claims 1-12 and 14-19 under 35 U.S.C. §103 is not proper. Accordingly, Appellant respectfully requests that the rejection of the pending claims 1-12 and 14-19 be overturned by the Board, and that the present patent application be allowed to issue as a patent with all pending claims.

Respectfully submitted,

Dated: 10/14/05

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DOCKET NO.: 10012773-1

VIII. APPEALED CLAIMS - APPENDIX

1. A SYNC pulse compensation apparatus, comprising:

a sampling compensation circuit operable to condition a SYNC pulse signal, wherein said SYNC pulse signal is based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion; and

a jitter cycle delay compensation circuit coupled to said sampling compensation circuit, said jitter cycle delay compensation circuit operating to tap said SYNC pulse signal after a predetermined delay based on a skew difference between said first and second clock signals.

2. The SYNC pulse compensation apparatus as set forth in claim 1, wherein said sampling compensation circuit comprises a plurality of multiplexers arranged in series, each multiplexer operating to receive an input through a timing register associated therewith.

3. The SYNC pulse compensation apparatus as set forth in claim 2, wherein said multiplexers are operable to insert a logic high condition in said SYNC pulse signal when said SYNC pulse signal is sampled to contain a plurality of logic lows during a predetermined time window.

4. The SYNC pulse compensation apparatus as set forth in claim 2, wherein said plurality of multiplexers comprises three multiplexers operable to insert a [010] sequence in said SYNC pulse signal when said SYNC pulse signal is sampled to be all zeros during a predetermined time window.

5. The SYNC pulse compensation apparatus as set forth in claim 1, wherein said jitter cycle delay compensation circuit comprises:

a series of delay registers, each operating to delay said SYNC pulse signal by a predetermined amount of time; and

a multiplexer operable to select a delayed SYNC pulse output generated from said series of delay registers.

6. The SYNC pulse compensation apparatus as set forth in claim 5, wherein said series of delay registers comprises eight registers.

7. The SYNC pulse compensation apparatus as set forth in claim 5, wherein said multiplexer is actuated by a JITTER-STATE control signal generated by a state/correct block responsive to said skew difference between said first and second clock signals.

8. The SYNC pulse compensation apparatus as set forth in claim 7, wherein said state/correct block is coupled to a phase detector operating to detect said skew difference between said first and second clock signals.

9. The SYNC pulse compensation apparatus as set forth in claim 7, wherein said JITTER-STATE control signal is stored in a flip-flop.

10. A SYNC pulse compensation method, comprising:

sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion; and

if said SYNC pulse signal is sampled to contain an anomalous condition during a predetermined time period, removing said anomalous condition by activating appropriate SYNC correct control logic.

11. The SYNC pulse compensation method as set forth in claim 10, wherein said second clock signal is generated by a phase-locked loop (PLL) based on said first clock signal.

12. The SYNC pulse compensation method as set forth in claim 10, wherein said SYNC pulse signal is generated when a rising edge in said first clock signal coincides with a rising edge in said second clock signal.

14. A SYNC pulse compensation method, comprising:

sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion;

determining a clock state indicative of a phase difference between said first and second clock signals;

re-positioning said SYNC pulse signal based on said clock state; and

if said SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state.

15. The SYNC pulse compensation method as set forth in claim 14, wherein said SYNC pulse signal is re-positioned by adding at least an extra clock cycle when said clock state indicates that said first clock signal lags with respect to said second clock signal by a predetermined amount.

16. The SYNC pulse compensation method as set forth in claim 14, wherein said SYNC pulse signal is re-positioned by deleting at least an extra clock cycle when said clock state indicates that said second clock signal lags with respect to said first clock signal by a predetermined amount.

17. The SYNC pulse compensation method as set forth in claim 14, wherein said SYNC pulse signal is delayed by propagating said SYNC pulse signal through a series of delay registers operable to be selected by a multiplexer in response to a JITTER-STATE control signal corresponding to said clock state.

18. The SYNC pulse compensation method as set forth in claim 17, wherein said JITTER-STATE control signal is stored in at least one flip-flop.

19. The SYNC pulse compensation method as set forth in claim 14, wherein said first and second clock signals comprise a core clock and a bus clock, respectively, in a computer system.

DOCKET NO.: 10012773-1

IX. EVIDENCE - APPENDIX

None.

DOCKET NO.: 10012773-1

X. RELATED PROCEEDINGS - APPENDIX

None.